Challenges in Developing an Integrated Electronic Neuro Prosthetic Implantable System for the Brain

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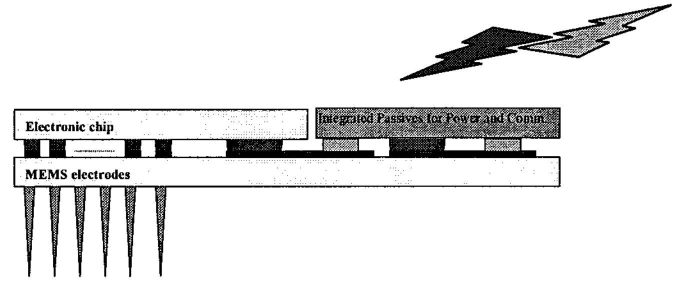
Outline

- **Review of the Miniaturization Goals**
- **Technical Approach**
- **Challenges and Issues**
- **Plan and Timetable**
- **The Team & Collaborative Work Flow**

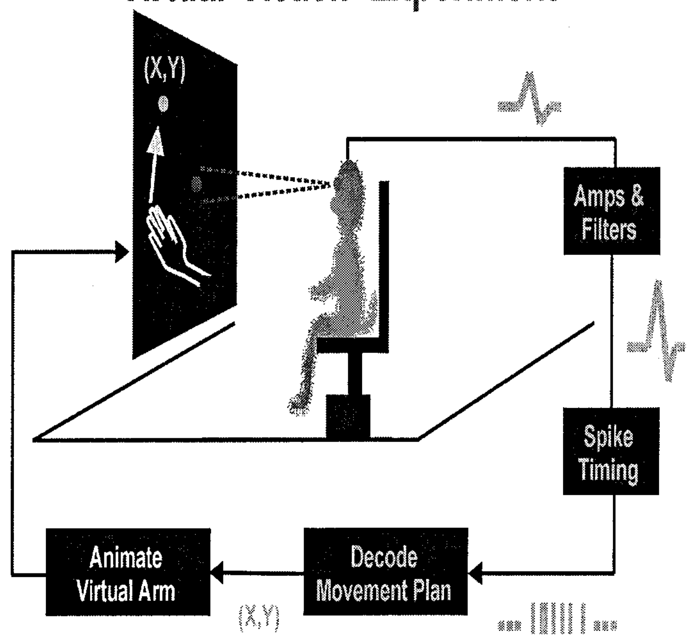
Program Goals

- **Our goal is to develop a fully miniaturized implantable neuro-prosthetic system consisting of integrated electronics and the Micro Electro Mechanical Structure (MEMS) base electrode array that has the following characteristics:**
  - **Can extract signals from brain neurons**
  - **Can provide on chip conditioning and processing of the extracted data**
  - **Can be programmed through a wireless link**
  - **Can transmit data through wireless link to a remote station**
  - **Can be self powered or powered through a wireless link**



Cross section of the final assembled device

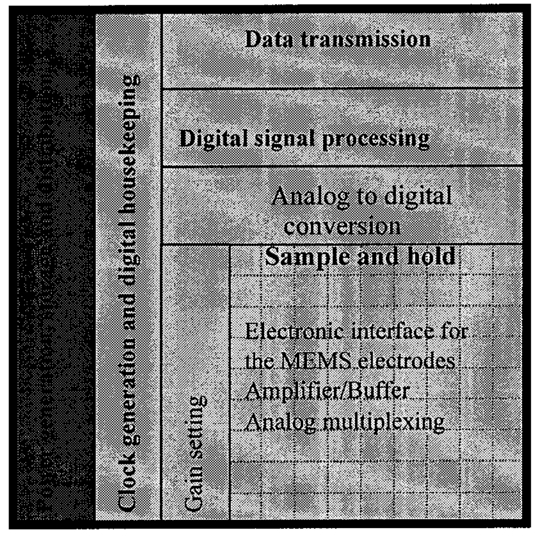
Virtual Reach Experiment



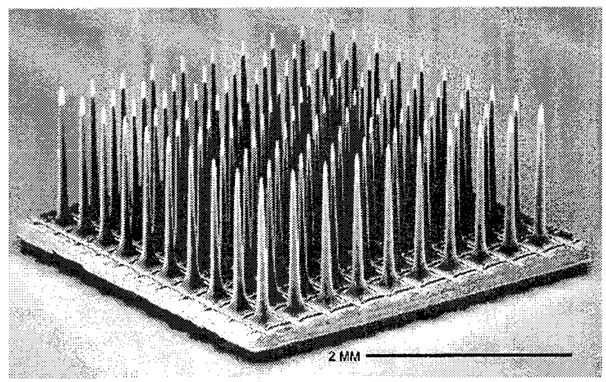
Technical Approach

① **Concentrate on the design of integrated ultra low power data acquisition electronic chip**

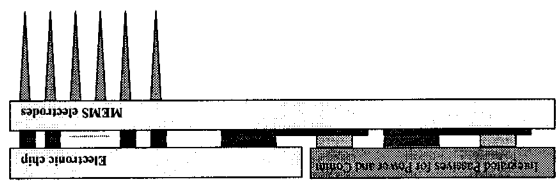
- **Phase 1, multiplexing chip to reduce the number of wires**
- **Phase 2, add ADC and DSP to condition the data**
- **Phase 3, add wireless link and develop completely wireless chip**



② **Leverage existing Micro Electro Mechanical Structure (MEMS) based passive probes**



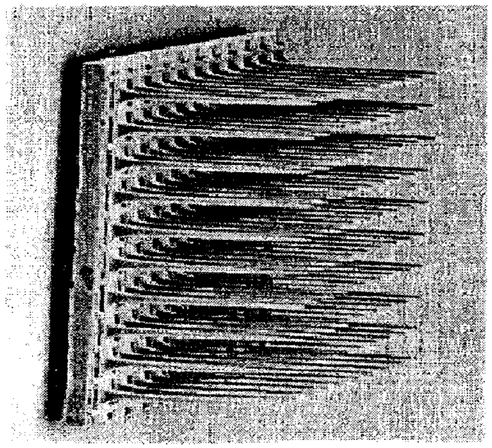
③ **Utilize "heterogeneous" integration techniques for merging the MEMS and electronics to build the neuro-prosthetic implant system**

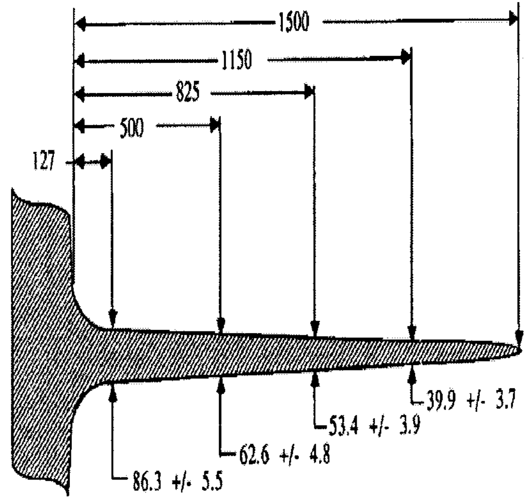


Cross section of the final assembled device

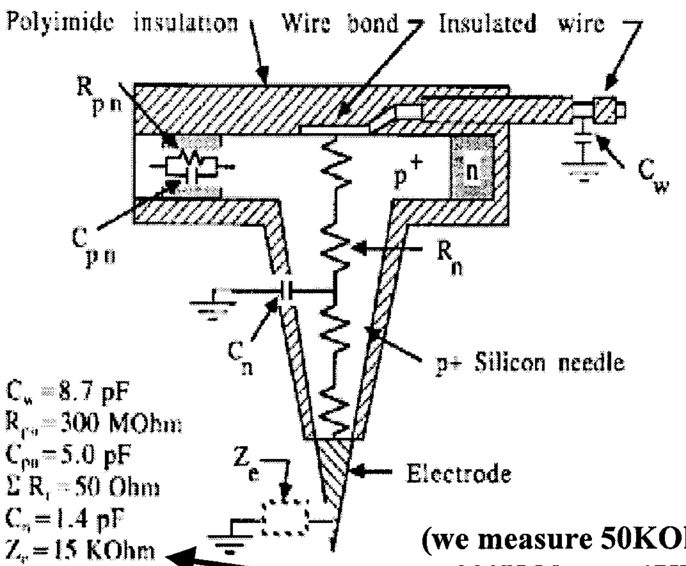
Characteristics of the MEM Device

- The MEMS electrode array consists of 100 electrodes micro machined on a silicon substrate
- Each electrode terminates to its own pad and needs a wire
- 100 wires are needed for getting signals from all electrodes
- Electrical Characteristics:



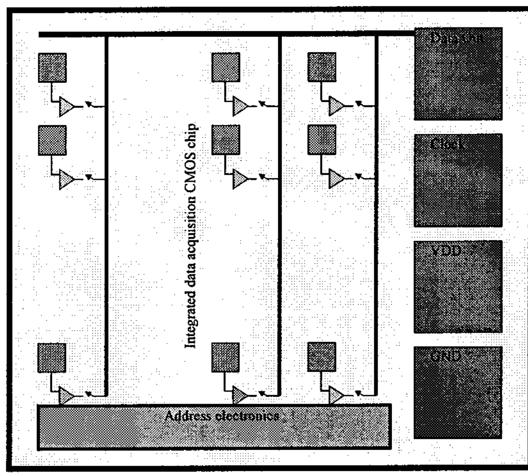


P. Campbell, et al, IEEE Transaction on Biomedical Engineering, Vol. 38, No.8 Aug 1991



(we measure 50KOhm to 300KOhm at 1KHz)

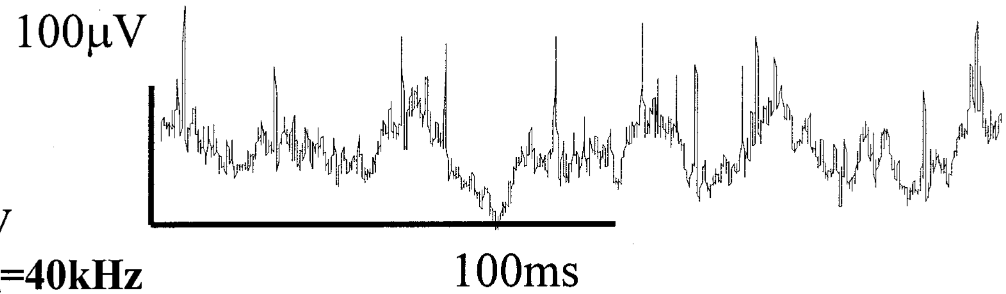
P. Campbell, et al, IEEE Transaction on Biomedical Engineering, Vol. 38, No.8 Aug 1991



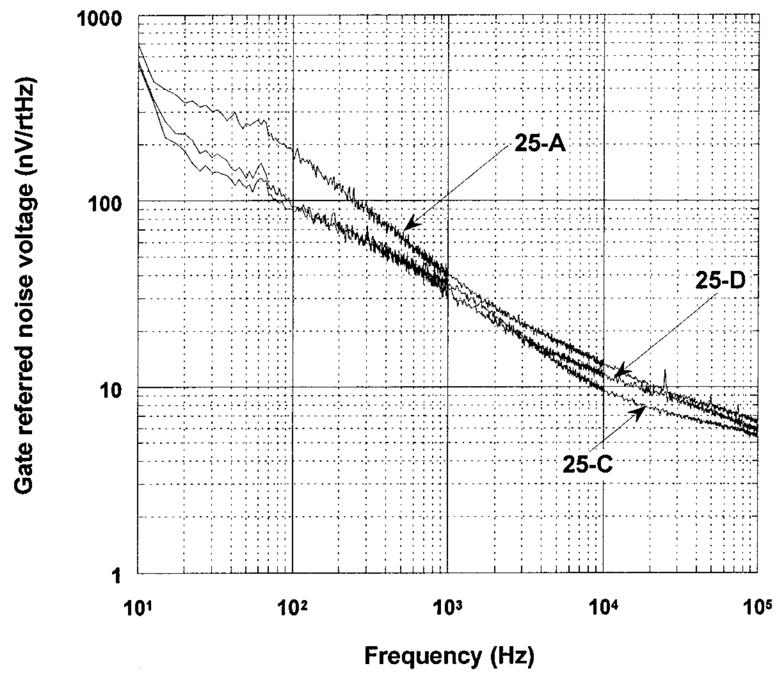
Data Acquisition Chip with multiplexing circuits reduces the number of wires to 4 and allows 100% "visibility" for all electrodes

- For heterogeneous integration the chip will use a matrix of micro-pads with exact "foot print" as the pads in the MEMS array

Challenges: Integrating Ultra Low Power Data Acquisition Chip

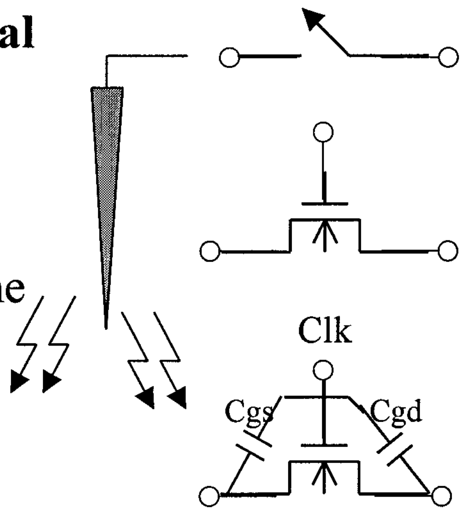


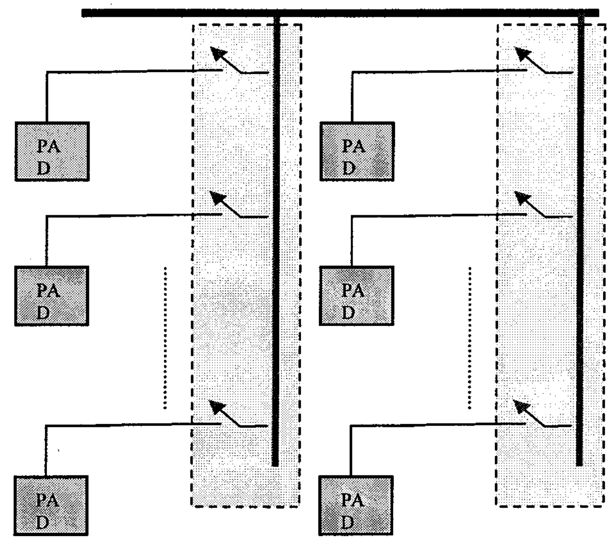
- **The signal are very small:**
  - **Spikes;** **Amplitude=30 μV to 300 μV**
    Width=1 millisecond, f_{sample}=40kHz
  - **Local field** **A=10μV to 100 μV**
    f=1Hz to 200 Hz
- **Large frequency dependent "flicker" noise in low power CMOS:**
  - **Noise can be reduced by increasing the size of the transistors and the bias current**
  - **Increasing bias current increases power**
- **Power:**
  - **Chip temperature rise< 2 deg. F may cause permanent damage to the brain cells**
  - **Total power dissipation< 10mWatts**



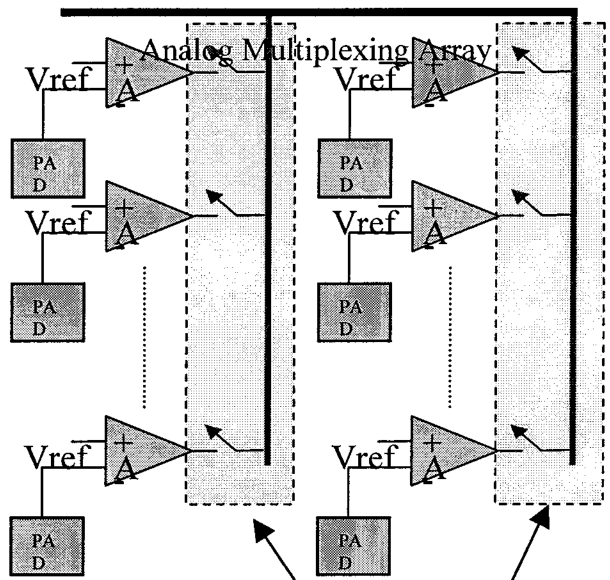
Challenges: Data Extraction and On Chip Multiplexing

- **Charge injection on traditional CMOS switch; discharge of parasitic capacitors may:**
  - Stimulate the brain cells
  - Cause rapid corrosion of the electrodes



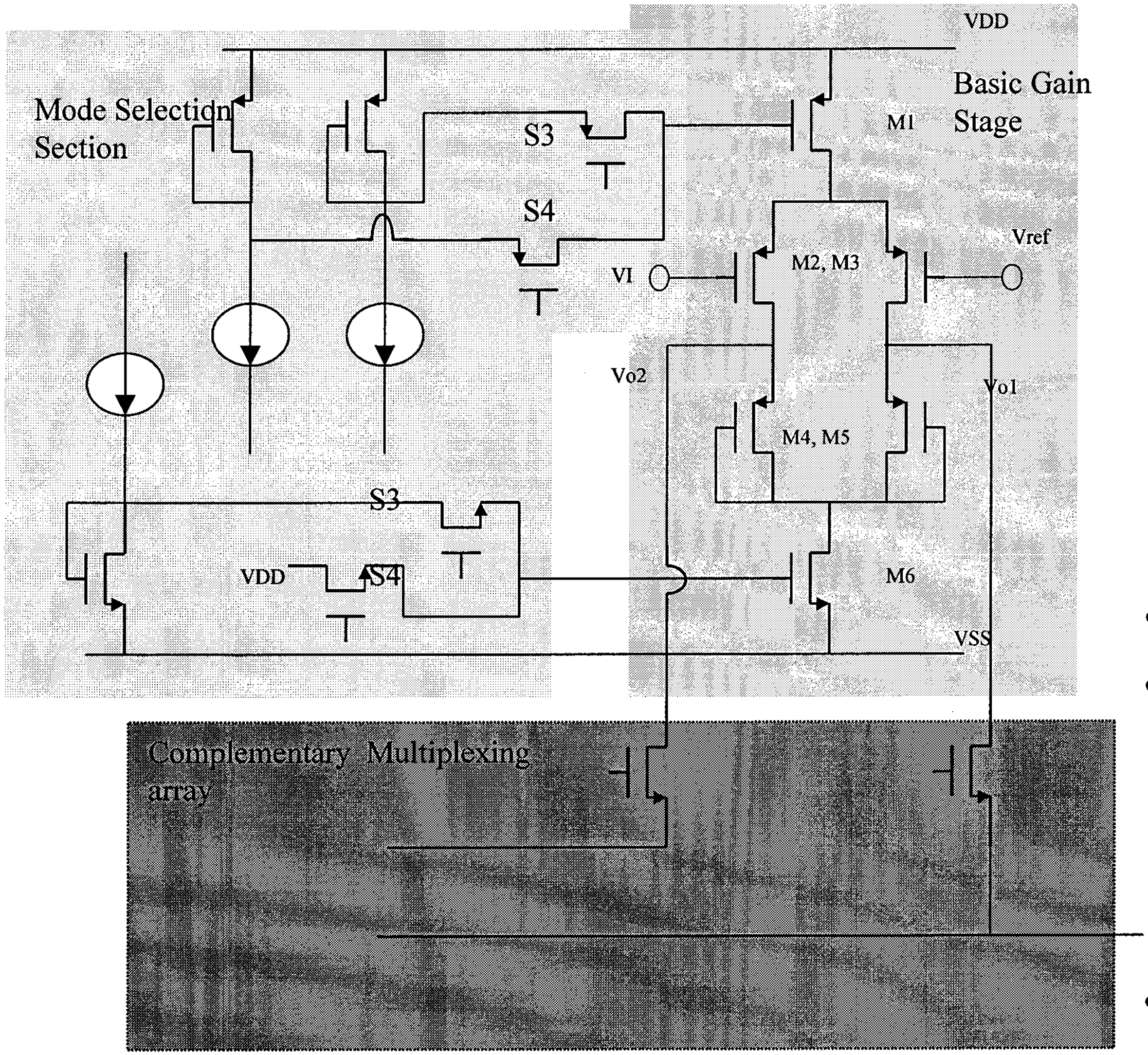


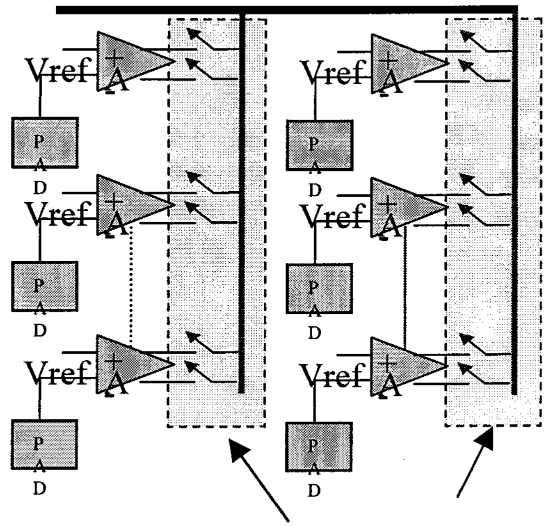
- **Buffering and amplification signal**
  - Uniform gain
  - Temperature stability
  - Very low power



Analog Multiplexing Array

Possible Basic Cell

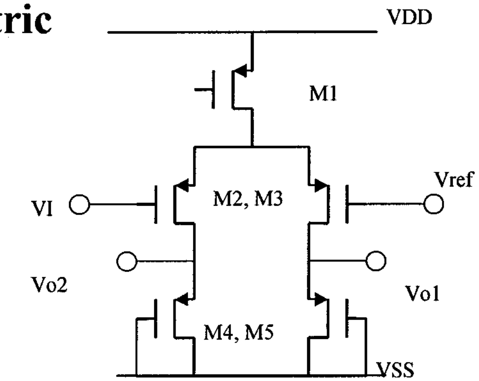


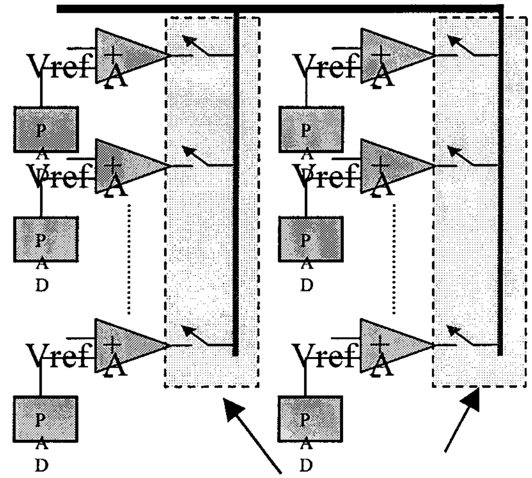


- **Low power CMOS design**
- **Dual mode gain stage:**
  - High acquisition bias current to minimize noise
  - Very low total power consumption
- **Differential multiplexing**
- **Enhanced SNR**

Challenges: On Chip Amplification and Power Management

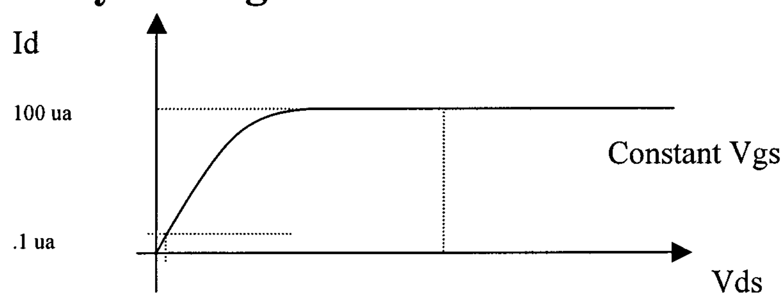
- **Amplification of signal**
  - **Modest fixed gain set by geometric factors $(W/L)_2/(W/L)_4$**
  - **Temperature independent**
  - **Differential output**

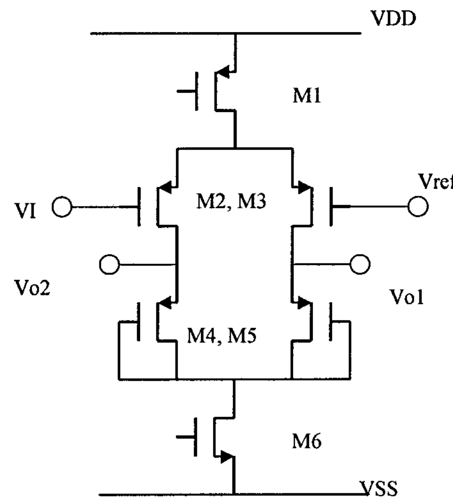




Analog Multiplexing Array

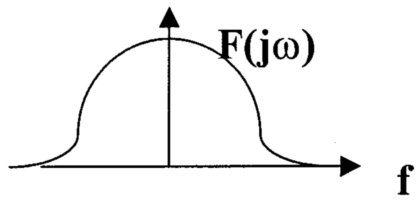
- **Needs bias current**
- **May need an additional shared gain stage after the multiplexing switches**
- **Use active power management; switch amplifier on only during the data measurement cycle**
- **M6 prevents injection of charges back into the electrode array during the switching**



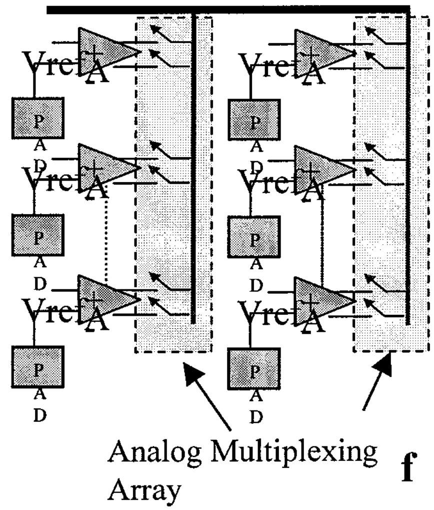


Challenges: Data Sampling & Analog to Digital Data Conversion

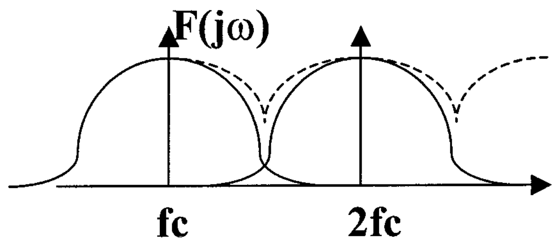
- **Use time division multiplexing**
  - **100 channels @ 20 KHz results fc>=4MHz**



Before Sampling



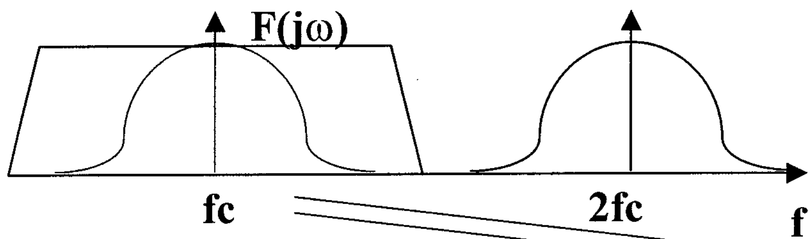
- **Multiplexing causes aliasing**



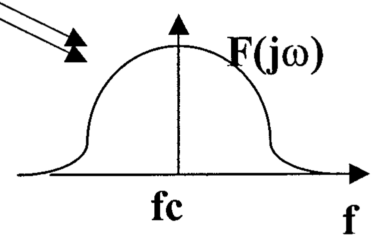
After Sampling

- **May need one Anti Aliasing Filter (AAF) per channel**
  - **Low frequency filter**
  - **Large capacitors**

- **Over-sampling &AAF**
  - **Single higher frequency filter**
  - **Smaller capacitors**

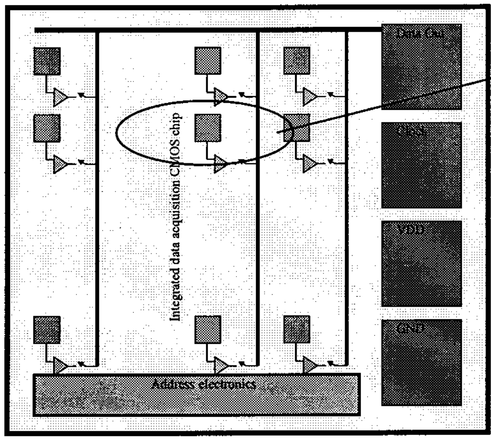


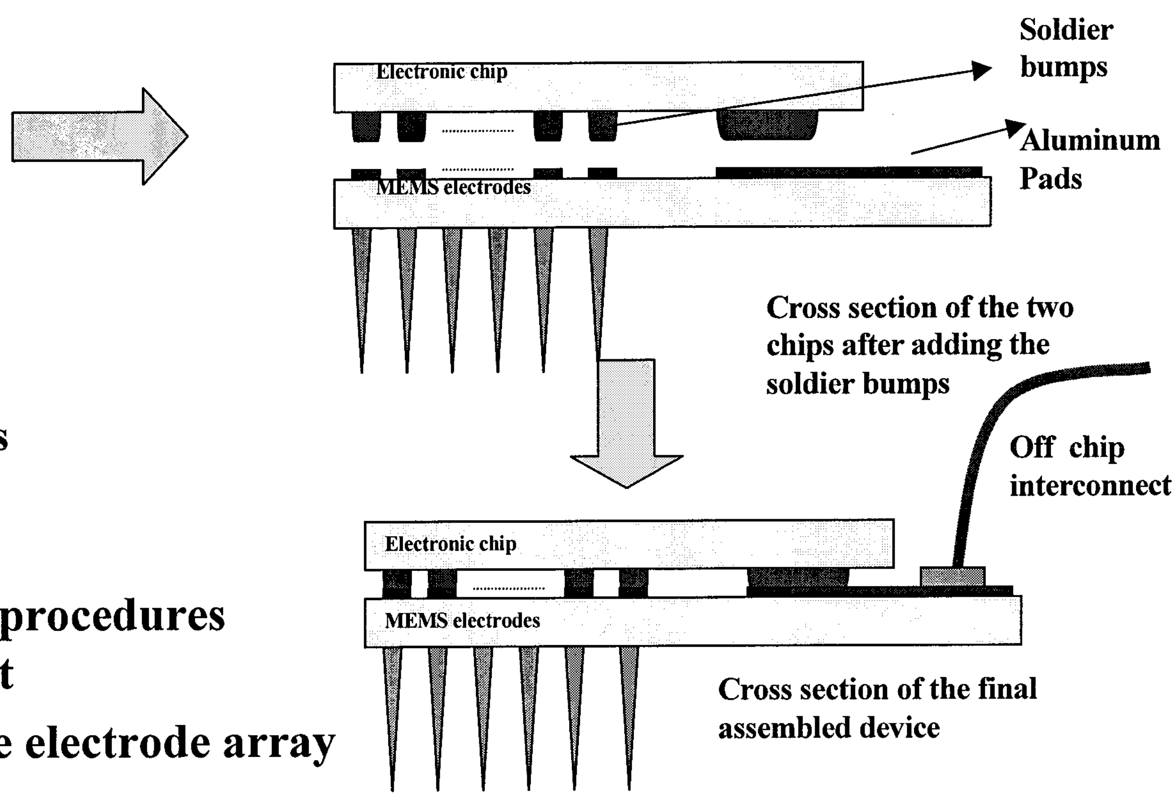
Over-sampling and AAF



After AAF

Challenges: Heterogeneous Integration





- **Redesign of the passive array**
  - **Add extension for crossovers**
  - **Add ground/seal ring**
- **Flip chip-to-chip attachment procedures including fine pitch alignment**
- **Preserving the integrity of the electrode array during the assembly**
- **Under-filling of the interface layer**
- **Material compatibility with biological tissue**

The Design Team

JPL :

Mohammad M. Mojarradi (PMAD)
Brent Blaes (Mixed Signal Design)
Bedabrata Pain (ADC)
Monico Ortiz (Mixed Signal Design)
Amin Mottiwala (Advanced Packaging)

University Team

Bill Kuhn (Professor, Kansas State University)
RF circuit design and wireless link
David Binkley (Professor, University of N. Carolina)
Extremely low power circuits
Jeff Young (Professor, University of Idaho)
Micro antenna design

Development Plan

- **Years 1 &2:**

  Prototype 1st generation smart neuro-prosthetic system

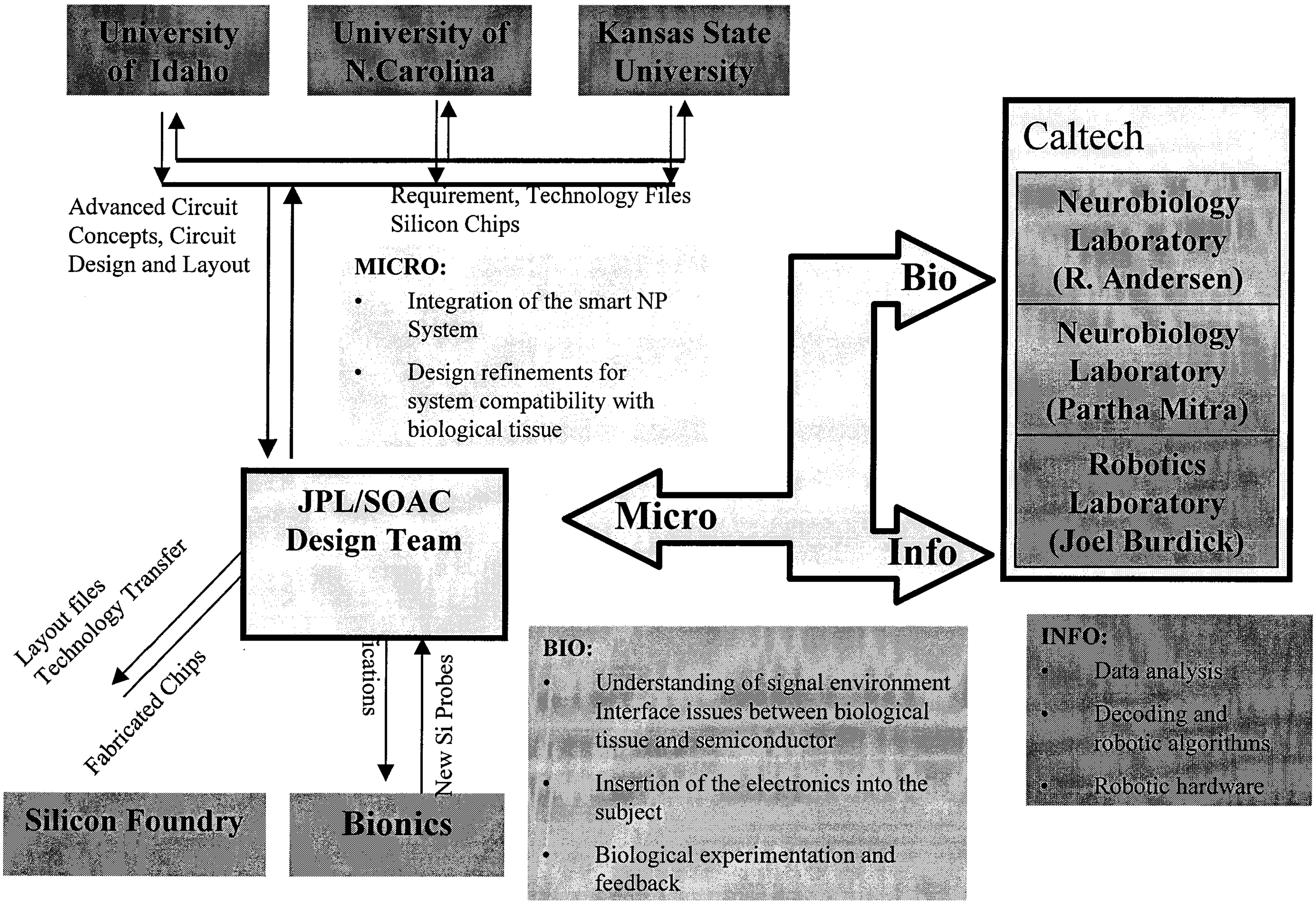
  Reduce # of wires, provide 100% access to all electrodes, enhanced SNR

- **Years 2 & 3:**
  - **Prototype 2nd generation neuro-prosthetic system**

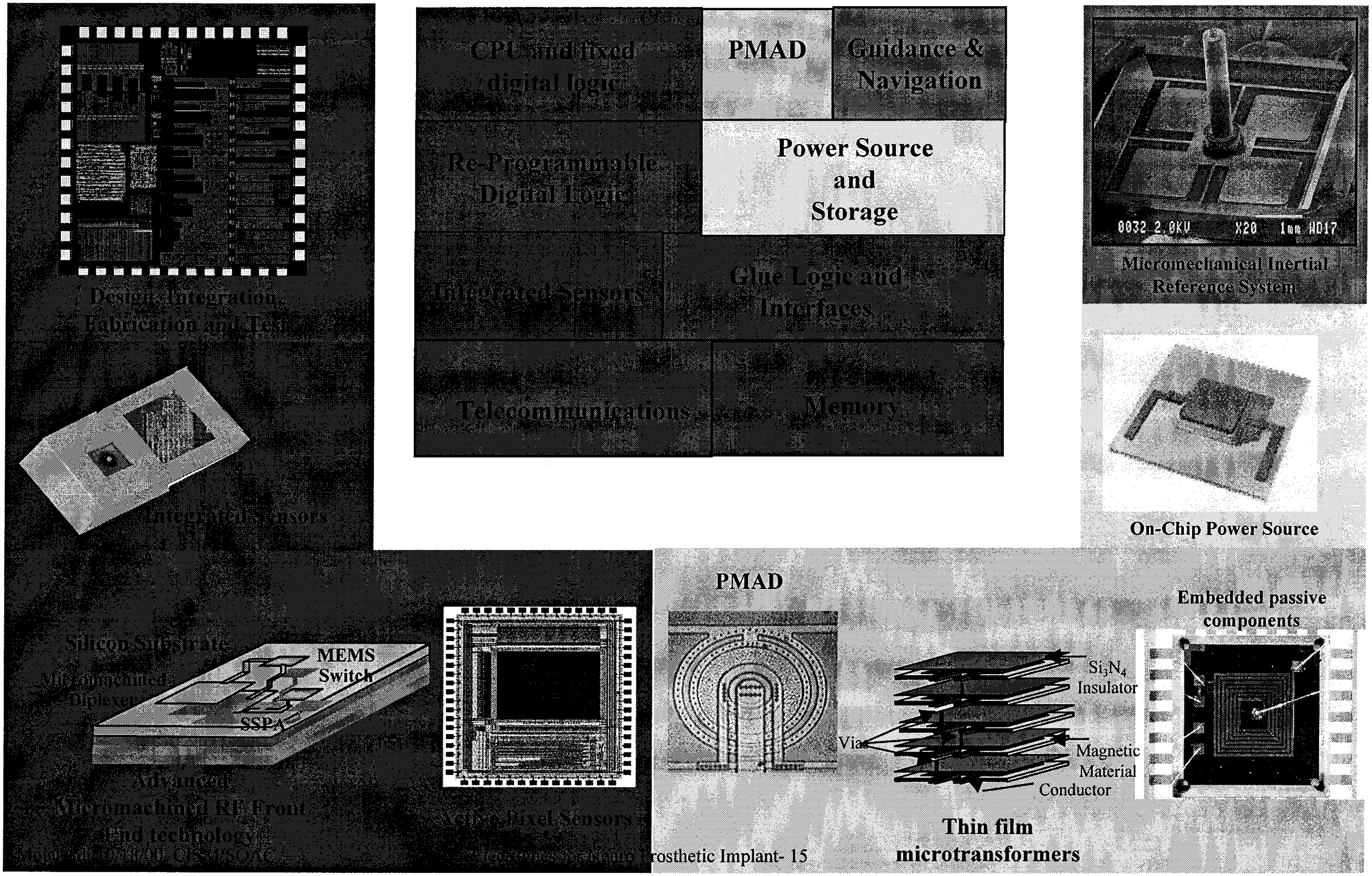
    Data conditioning, analog to digital conversion, digital signal processing

- **Years 3 to 5:**
  - **Develop 3rd generation completely wireless neuro-prosthetic system**

Collaborative Work Flow



NASA SOAC-Technology



Leveraging NASA SOAC Technologies

- **Univ. of Idaho: Harry Li**
  High Voltage Transistors on SOI CMOS, High Voltage Modeling and Mixed Voltage Circuit Building Blocks
- **Mississippi State Univ.: Ben Blalock**
  Analog circuits in SOI CMOS, Mixed signal primitive blocks in SOI CMOS and Mixed signal circuits for PMAD
- **Kansas State Univ.: William Kuhn**
  Integrated High Frequency Transformers and Magnetically Coupled Data Isolators
- **University of Arkansas: Alan Mantooth**
  Integrated Sensor Interface and Thermally Coupled Data Isolator Circuits
- **University of Michigan Linda Katehi**
  RF MEMS